

REMARKS

The Final Office Action dated October 4, 2004 has been received and carefully considered. In this response, claims 1, 7-13, 20-23 and 25 have been amended to address various informalities and to remove reference to “step of” phrases. These amendments do not narrow the scope of the claims and no new matter is introduced by the amendments to the claims. Reconsideration of the outstanding rejections in the present application therefore is respectfully requested based on the following remarks.

Comments on Examiner's Remarks

At page 2, paragraph 4, of the Office Action, the Examiner states that the limitations of “common circuitry at an intermediate stage that can be selectively placed in one mode or another” is absent from the language of claim 1. The Applicants respectfully disagree with this characterization of the language of claim 1. Claim 1 recites the limitations of a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage; a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage; and dual mode sub-processing circuitry, *associated with each of said two-dimensional image pipeline and said three-dimensional image pipelines*, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations *associated with said two-dimensional image pipeline at an intermediate stage thereof* and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations *associated with said three-dimensional image pipeline at an intermediate stage thereof*. As will be appreciated, the dual mode sub-processing circuitry acts as “common circuitry” in that it is associated with each of the two-dimensional and three-dimensional image pipelines, it is operable to operate in the two-dimensional mode, whereupon it performs motion operations associated with an intermediate stage of the two-dimensional pipeline, or in the three dimensional mode, whereupon it performs rasterization operations associated with an intermediate stage of the three-dimensional pipeline. As such, the dual mode sub-processing circuitry comprises common circuitry as it may be used for either the two-dimensional image pipeline or the three-dimensional pipeline depending on its selected mode.

Obviousness Rejection of Claims 1-30

At page 3 of the Office Action, claims 1-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over DiNicola (U.S. Patent No. 5,394,524) in view of Ezer (U.S. Patent No. 6,275,239) and further in view of Herrera (U.S. Patent No. 6,208,350). This multi-tiered rejection is respectfully traversed.

As stated in MPEP § 2143, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Also, as stated in MPEP § 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Further, as stated in MPEP § 2143.01, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). That is, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970). Additionally, as stated in MPEP § 2141.02, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

Finally, if an independent claim is non-obvious under 35 U.S.C. 103, then any claim depending therefrom is non-obvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Claim 1, from which claims 2-6 depend, recites, in part, the limitations of a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space, a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space, and dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipelines, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry *performs motion compensation operations* associated with said two-dimensional image pipeline *at an intermediate stage thereof* and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs *rasterization operations* associated with said three-dimensional image pipeline *at an intermediate stage thereof*.

The Examiner asserts that DiNicola, Ezer, and Herrera, if combined as proposed, disclose these limitations. Specifically, the Examiner asserts that DiNicola discloses a 2D subsystem 301 that is purportedly analogous to the two-dimensional image pipeline of claim 1, a 3D processing node that is purportedly analogous to the three-dimensional image pipeline of claim 1, and an attribute processor (AP) 306 that is purportedly analogous to the dual mode sub-processing circuitry of claim 1. The Examiner admits that DiNicola “is silent about [the limitations of] wherein when in said two-dimensional mode said dual-mode processing circuitry performs operations associated with said two-dimensional image pipeline and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs operations associated with said three-dimensional image pipeline” as recited by claim 1. *Office Action*, p. 4. Accordingly, the Examiner relies on the teachings of Ezer as allegedly disclosing

a media coprocessor which supports 3-D graphics, video and audio. . . The media processor 102 performs different operations using its several functional units such as :digital [sic] signal processor 202 that performs 2D and 3D functions (co., 4, lines 1-16) thus disclosing similarity in circuit implementation that allows common circuitry to share functions associated with two- and three-dimensional

image pipelines and the seemingly different operation required thereby which is similarly recited in [claim 1].

Id.

The Examiner then concludes that “it would have been obvious to a person of ordinary skill in the art . . . to modify the ‘(attribute processor (AP) 306)’ with the feature ‘a media coprocessor that is able to provide an application spectrum . . .’ as taught by Ezer et al because it results in improved cost/performance to applications.” *Id.*

The Examiner also admits that the DiNicola fails to disclose or suggest the limitations of graphics operations associated with said two-dimensional image pipeline in one mode as recited by claim 1. The Examiner therefore turns to Herrera which purportedly discloses “using a graphics engine to generate digital image data based on at least one command similar to ‘one mode or another’ as per [claim 1] and the same graphics engine generating motion compensated digital image data base on at least one digital image map and at least one motion vector (col. 5, lines 5-67; col. 6, lines 1-11).” The Examiner therefore concludes that one of ordinary skill in the art would be motivated to modify the proposed combination of DiNicola and Ezer by the teachings of Herrera “because it provides a cost-effective solution for doing both 2D ad 3D processing in one system ([Herrera,] col. 6, lines 1-11; col. 13, lines 66-67; col. 14, lines 1-6).

As a first issue, the proposed combination of the teachings of DiNicola, Ezer and Herrera does not disclose or suggest every limitation of claim 1. As noted above, claim 1 recites the limitations of dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipelines, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry *performs motion compensation operations* associated with said two-dimensional image pipeline *at an intermediate stage thereof* and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs *rasterization operations* associated with said three-dimensional image pipeline *at an intermediate stage thereof*. The Examiner proposes the modification of the attribute processor 306 of DiNicola based on the media coprocessor 102 of Ezer to arrive at the dual mode sub-processing circuitry of claim 1. *Office Action*, p. 4.

However, it is respectfully submitted that such a modification would still fail to disclose the limitations of wherein the dual mode sub-processing circuit performs motion compensation operations associated with the two-dimensional image pipeline at an intermediate stage of the two-dimensional image line or performs rasterization operations associated with the three-dimensional pipeline at an intermediate stage of the three-dimensional pipeline. DiNicola teaches that

An attribute processor (AP) 306 performs preprocessing of the incoming 2D and 3D data streams (such as graphics attribute processing) and dispatches work to the 3D processing nodes 305 or to the 2D subsystem 301, as appropriate. Attribute processor 306 may be either a suitably programmed general-purpose processor or a special-purpose logic circuit.

Attribute processor 306 reads work from an input FIFO, memory or other input path and *moves work groups to the appropriate processing node 305*. This processor is also responsible for operations such as including a sequence number with the work groups so that the work groups may be reordered *after processing by the processing nodes 305*. Also, for some graphics data streams, the processor may perform display list processing and non-drawing processing.

Attribute processor 306 is utilized to parse or partition the 3D data stream into multiple segments in accordance with a preferred embodiment of the present invention. Each segment is also called a work group (WG), and each work group may contain one or more work elements. The number of work elements in a work group may be determined by various factors such as the amount of processing time that it takes to process a work group versus the amount of processing time it takes to group work elements into a work group. Attribute processor 306 is coupled to a RAM 308, which is employed to store various instructions or data utilized by attribute processor 306. Additionally, attribute processor 306 may move data by utilizing other devices such as DMA controllers, processors, or with internal features within the attribute processor itself. Attribute processor 306 may perform graphics processing and supply current attribute data to the processing nodes 305 along with the work to be done.

DiNicola, col. 5., line 55 – col. 6, line 21 (emphasis added).

It will be appreciated from the above-cited passage that the attribute processor 306 “performs preprocessing of the incoming 2D and 3D data streams (such as graphics attribute processing).” One of ordinary skill in the art will appreciate that the preprocessing of incoming 2D and 3D data streams by the attribute processor 306 as described by DiNicola does not disclose, imply or suggest that the attribute processor 306 could be modified to perform motion compensation operations or rasterization operations in view of the teachings of Ezer as these operations are conventionally viewed as core image processing operations and therefore do not

fall into the “preprocessing” of incoming 2D and 3D data streams as DiNicola attributes to the attribute processor 306. Moreover, the modification of the attribute processor 306 to perform actual image processing operations would destroy the parallel 2D/3D data stream processing goal of DiNicola as the processing of each data stream would have to rely on the attribute processor 306 as a single, shared component, which could introduce a delay in processing which DiNicola seeks to avoid.

Even if it is assumed, *arguendo*, that the attribute processor 306 could be so modified without destroying the functionality of DiNicola, such a modification would not disclose or suggest the performance of motion compensation operations or rasterization operations at intermediate states of the two- and three-dimensional image pipelines as recited by claim 1. As disclosed by DiNicola, the attribute processor 306 functions *prior to the initial stages* of the 2D subsystem 301 and 3D processing node 305 which the Examiner asserts are analogous to the two-dimensional and three-dimensional image processing pipelines, respectively, of claim 1. There is no support for the modification of the attribute processor 306 to perform graphics operations at intermediate stages of the 2D graphics subsystem 301 or the 3D graphics nodes 305 as DiNicola provides no disclosure or suggestion that any communications occur between elements 301, 305 and 306 at the intermediate stages nor does DiNicola provide any disclosure enabling such communications.

As a second issue, the Applicants respectfully submit that there is no motivation to combine the teachings of DiNicola, Ezer and Herrera as proposed by the Examiner, regardless of whether such combination discloses the limitations of the claims. The Examiner merely provides general statements of motivation such as “improved cost/performance to applications” and “a cost-effective solution for doing both 2D and 3D processing in one system.” Allegations of improved cost and performance, without specifically describing how the proposed combination of teachings would achieve these goals, are insufficient demonstrations of motivation for one of ordinary skill in the art to combine the teachings. Moreover, the Applicants respectfully submit that the proposed combination of DiNicola, Ezer and Herrera is contrary to the teachings of DiNicola, Ezer and Herrera. DiNicola teaches that

Systems which are currently on the market providing 2D and 3D data stream support *process these data streams sequentially, i.e., by time-multiplexing them on a single processor or processor complex*. They process one data stream for a

period of time, then they process the second for a period of time, and then they return to the first. *This approach is an unacceptable solution since intermixing a data stream which is computationally intensive with one that is highly interactive generally degrades both.* The computationally intensive one (3D) does not get as much processor time as it might, and the interactive one (2D) must wait for the 3D data stream to be processed before getting an opportunity to display the interactive information that the user is waiting for. Currently available systems require large amounts of context information to be swapped in order to switch from processing 3D information to processing 2D information and back. . . . However, *the traditional approach of time-slicing between the two types of datastreams can cause serious performance problems*, as noted above.”

DiNicola, col. 1, line 53 – col. 2, line 10 (emphasis added).

As demonstrated by the above passage, *DiNicola* teaches that the sequential processing (i.e., time-multiplexing) of a 2D data stream and a 3D data stream is “an unacceptable solution.” To overcome this “unacceptable solution,” *DiNicola* teaches a system whereby a 2D data stream and a 3D data stream are “processed concurrently (i.e., in parallel) in such a manner that processing of the 2D data stream is not held up by processing of the 3D data stream.” *Id.*, Abstract. In contrast, the invention of Ezer “relates to an integrated media coprocessing chip which partitions 3-D graphics, video, and audio tasks *through time division multiplexing.*” *Ezer*, col. 2, lines 10-13; *see also Ezer*, col. 1, line 67-col. 2, line 2 (“With the media co-processor chip, the present invention partitions different media tasks *so that they are performed sequentially in a time-division multiplexed format*”). *Ezer* teaches that the motivation for the sequential performance of different media tasks is to “provide a much less expensive computing system without sacrificing much in the way of functionality, quality and versatility. The present invention achieves this by designing a single, integrated media co-processor chip which is capable of processing graphics, video and audio. *This reduced costs because it minimizes duplicate functionalities and redundant circuitry.*” Thus, whereas *DiNicola* seeks improved performance by adding additional, duplicative and redundant circuitry (and thereby increasing the complexity and cost) so that 2D and 3D data streams can be processed in parallel to improve performance, *Ezer* teaches the reduction of additional, duplicative functionalities and redundant circuitry so as to reduce cost. As such, the approaches of *DiNicola* and *Ezer* are diametrically opposed and it therefore will be appreciated that the modification of the teachings of *DiNicola* by the teachings of *Ezer* to allegedly arrive at the limitations of claim 1 is contrary to both the improved performance/duplicative circuitry approach of *DiNicola* and the reduced cost/reduced

circuitry approach of Ezer and therefore would destroy both of their respective advantages. Accordingly, one of ordinary skill in the art, considering the teachings of DiNicola and Ezer in their entirety, would find no motivation to combine their teachings as proposed by the Examiner.

Claim 7, from which claims 8-13 depend, recites the similar limitations of *performing motion compensation operations* associated with said two-dimensional image pipeline *at an intermediate stage thereof using said dual-mode sub-processing circuitry* in said two-dimensional mode and *performing rasterization operations* associated said three-dimensional image pipeline *at an intermediate stage thereof using said dual-mode sub-processing circuitry* in said three-dimensional mode. As discussed above with reference to claim 1, there is no motivation to combine the teachings of DiNicola, Ezer and Herrera as proposed by the Examiner, and even if so combined, the proposed combination of DiNicola, Ezer and Herrera fails to disclose or suggest at least these limitations and therefore fails to disclose or suggest each and every limitation of claim 7.

Claim 14, from which claims 15-19 depend, recites the similar limitations of dual mode sub-processing circuitry, associated with each of said two-dimensional and said three-dimensional image pipelines, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof and a controller that is operable to control said dual mode sub-processing circuitry to perform said motion compensation operations in said two-dimensional mode and to perform said rasterization operations in said three-dimensional mode. As discussed above with reference to claim 1, there is no motivation to combine the teachings of DiNicola, Ezer and Herrera as proposed by the Examiner, and even if so combined, the proposed combination of DiNicola, Ezer and Herrera fails to disclose or suggest at least these limitations and therefore fails to disclose or suggest each and every limitation of claim 14.

Claim 20, from which claims 21-25 depend, recites the similar limitations of controlling said dual mode sub-processing circuitry to perform either motion compensation operations

associated with said two-dimensional image pipeline at an intermediate stage thereof in said two-dimensional mode, or rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof in said three-dimensional mode. As discussed above with reference to claim 1, there is no motivation to combine the teachings of DiNicola, Ezer and Herrera as proposed by the Examiner, and even if so combined, the proposed combination of DiNicola, Ezer and Herrera fails to disclose or suggest at least these limitations and therefore fails to disclose or suggest each and every limitation of claim 20.

Claim 26 recites the similar limitations of dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipeline, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof. As discussed above with reference to claim 1, there is no motivation to combine the teachings of DiNicola, Ezer and Herrera as proposed by the Examiner, and even if so combined, the proposed combination of DiNicola, Ezer and Herrera fails to disclose or suggest at least these limitations and therefore fails to disclose or suggest each and every limitation of claim 26.

Claim 27, from which claims 28-30 depend, recites the similar limitations of dual mode sub-processing circuitry operable in a selected one of first and second modes wherein in said first mode said dual-mode sub-processing circuitry forms an intermediate stage of said first specialty pipeline and in said second mode said dual-mode sub-processing circuitry forms an intermediate stage of said second specialty pipeline. As discussed above with reference to claim 1, there is no motivation to combine the teachings of DiNicola, Ezer and Herrera as proposed by the Examiner, and even if so combined, the proposed combination of DiNicola, Ezer and Herrera fails to disclose or suggest at least these limitations and therefore fails to disclose or suggest each and every limitation of claim 27.

In view foregoing, it is respectfully submitted that the Office Action fails to establish that the cited references disclose or suggest, alone or in combination, each and every limitation of

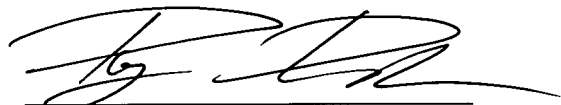
claims 1, 7, 14, 20, 26 and 27, as well as each and every limitation of claims 2-6, 8-13, 15-19, 21-25 and 28-30 at least by virtue of their dependency from one of claims 1, 7, 14, 20 and 27. Moreover, these claims recite additional limitations neither disclosed nor suggested by the cited references. It therefore is respectfully submitted that the obviousness rejection of claims 1-30 is improper at this time and withdrawal of this rejection therefore is respectfully requested.

Conclusion

The Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 01-0365.

Respectfully submitted,



Ryan S. Davidson, Reg. No. 51,596,
Filed under 37 C.F.R. 1.34(a)

Agent for Applicants

TOLER, LARSON & ABEL, L.L.P.

5000 Plaza On The Lake, Suite 265

Austin, Texas 78746

(512) 327-5515 (phone) (512) 327-5452 (fax)

6 December 2004
Date